Direzione Innovazione
e Internazionalizzazione

UNIVERSITÀ
DI TORINO

ID

VP055_INF

Visiting Professor Program
Academic Year 2024/2025

TEACHING COMMITMENT: **12 hours**

COURSE TITLE

Energy-Efficient Neural Architectures for Image Analysis and Video Coding

TEACHING PERIOD

2nd term

SCIENTIFIC AREA

Video compression for digital communication

LANGUAGE USED TO TEACH

English

COURSE SUMMARY

Over the past years, the deep learning paradigm has enjoyed increasing successes in fields related to image analysis and video coding. Such achievements come however at the price of increased memory requirements and computational complexity with respect to traditional algorithms. This is especially an issue in user devices such as mobiles, where resources are limited. In cloud environments, these requirements translate into increased energy consumption. So, for the deep learning paradigm to be profitably applicable to image analysis and video coding, resource- and energy-efficient implementations are required. Hardware implementations over FPGAs or ASICSs have recently shown to be able to reduce the energy consumption of these algorithms to a point where they become practical. This course aims at providing the foundations on the methods and tools enabling to implement energy efficient neural network based algorithms for image analysis and video coding tasks.

LEARNING OBJECTIVES

At the end of the course the student should be able to analyze neural network based image processing algorithms, identify the main sources of memory and computational complexity of an algorithm, define throughput requirements, suggest hardware-oriented optimizations and propose energy-efficient hardware architectures including processing units and memory hierarchies.
It is desirable that the course includes at least one of the following practical activities:

Processing units design: Register-Transfer Level (e.g, using VHDL/Verilog targeting FPGA);

Processing units design: High-Level Synthesis (e.g, using Intel HLS or Xilinx Vivado, depending on the platform available);

Memory hierarchy modeling and design (e.g., using CACTI and NVSIM);

Energy/Power analysis (e.g., using Intel Quartus Prime or Vivado power analyzer).

OTHER ACTIVITIES BESIDES THE COURSE

It is desirable that the visiting professor organizes at least one seminar addressed to the PhD students of the conferences and participates to the research activities of the host group.

VISITING PROFESSOR PROFILE

The sought profile shall have a strong background in energy-efficient implementations of algorithms for image analysis over FPGAs and ASICs. The sought profile shall also include proven hands-on experience with standardized coding technologies such as, for example, H.264, MVC, SVC, HEVC, 3D-HEVC, VVC, AV1. It is also very desirable that the profile includes skills in techniques for efficient deep learning for video prediction.

CONTACT REFERENT

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